DESIGN AND SIMULATION OF NESTED MULTILEVEL TOPOLOGIES

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Abstract- This project deals with design and simulation of multilevel topology based on the concept of nested arrangement. It has the advantages of reduced number of diodes and consequently gives higher efficiency as compared to the equivalent neutral point clamped inverter (NPC) topology. This method presents an optimized pulse width modulation strategy that provides synthesizing voltage waveforms with higher quality, and losses comparison with NPC topology. The simulation of Nested multilevel topology is to be done for 4, 5&6 levels and performance is to be compared in terms of total harmonic distortion (THD). Also, the PMSM motor is to be fed with this nested multilevel converter with different output voltage levels and performance comparison is to be accomplished in terms of torque ripples. The simulation is performed using MATLAB/Simulink software.

Keywords- DC-AC power converters, multi-level inverters, power electronics, pulse width modulation technique, permanent magnet synchronous motor.

I. INTRODUCTION
A multilevel converter [3] not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel converter system for a high power application. The concept of multilevel converters has been introduced since 1975. The term multilevel began with the three-level converter. Subsequently, several multilevel converter topologies have been developed. However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected. A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM). The attractive features of a multilevel converter can be briefly summarized as follows.

● Staircase waveform quality: Multilevel converters [2] not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses; therefore electromagnetic compatibility (EMC) problems can be reduced.
Common-mode (CM) voltage: Multilevel converters[9] produce smaller CM voltage; therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. Furthermore, CM voltage can be eliminated by using advanced modulation strategies such as that proposed in.

- Input current: Multilevel converters[14] can draw input current with low distortion.
- Switching frequency: Multilevel converters[7] can operate at both fundamental switching frequency and high switching frequency PWM.

It should be noted that lower switching frequency usually means lower switching loss and higher efficiency. Unfortunately, multilevel converters do have some disadvantages. One particular disadvantage is the greater number of power semiconductor switches needed. Although lower voltage rated switches can be utilized in a multilevel converter[8], each switch requires a related gate drive circuit. This may cause the overall system to be more expensive and complex. Multilevel inverters[9] give higher power. They are operated through multiple switches instead of one. They can use environmental friendly energies like wind and solar energy and convert them to AC.

When compared with an induction servo motor, a PMSM also has many advantages. For instance, it has the higher efficiency, resulting from the absence of rotor losses and lower no-load current below the rated speed. In addition, its decoupling control performance is far less sensitive to the parameter variations of the motor. To achieve fast four-quadrant operation, smooth starting, and acceleration, the field oriented control, or vector control, is used in the design of the PMSM drive. Much research has devoted fresh attention to the control of the PMSM.

Multilevel Converters[2] has been attracted a large interest in the power industry in the recent years. Industry has started to involve in higher power equipment, which already reaches megawatt level. Conventional power electronic converters are only able to switch each individual output link between two possible voltage levels, especially those of the internal DC voltage link. The general structure of the multilevel converter[8] is to generate a sinusoidal voltage from several levels of voltages which are usually obtained from capacitor voltage sources.

Three different topologies have been projected for multilevel converters:

- Diode clamped converter;
- Flying capacitor converter (Capacitor Clamped)
- Cascaded converter.

This paper investigates multilevel topologies[2] based on the concept of nested arrangement. Such topologies are called nested multilevel converters[15] because the central point of the legs are connected at the same point, with the external leg involving the internal one, as observed in Fig. 1. Fig. 1(a)–(c) shows the nested multilevel configuration with four, five & six levels.

An auxiliary resonant pole is applied through the nested three and five levels[19-21]. This nested multilevel topologies is applied four level to n level. When compared to NPC topologies, the studied configurations can be considered as an interesting option for applications that demand a number of levels higher than or equal to four, since as far as the number of levels increase higher is the reduction on the number of diodes employed. This paper also PMSM motor is to be fed with this nested multilevel converter with different output voltage levels and performance comparison is to be accomplished in terms of speed and torque ripples.
The effort in semiconductor cost is 550kVA, compared with 630kVA for the Neutral Point Clamped topology\cite{1}, but the components of the NPC\cite{4} will stay cooler so that they could be used at higher currents. In a comparison of maximum output power at 16kHz, the NPC module will be lower in cost than the module for a standard half-bridge, but with the need for a total semiconductor rating of 810kVA compared to 630kVA. Efficiency is becoming increasingly important in power electronics. Many applications are driven by the initiatives for reduced energy consumption. The technology leaders are inverter applications in the solar market, but also uninterruptible power supplies and motor drives have new targets for improved efficiency.

![Nested multilevel configurations with (a) four level, (b) five level, and (c) six level.](image)

**II. CONVERTER DESCRIPTION**

Each converter’s leg in Fig. 1(a) is constituted of two controlled switches (Sx1 and Sx4) and two bidirectional controlled switches (Sx2 and Sx3) with x=a, b, c. Table I shows the Pole voltage as a function of the switching states.
TABLE 1
Pole voltage as a function of the switching states

<table>
<thead>
<tr>
<th>$S_{x1}$</th>
<th>$S_{x2}$</th>
<th>$S_{x3}$</th>
<th>$S_{x4}$</th>
<th>$V_{x0}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>$V_{dc1}+(V_{dc2}/2)$</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>$V_{dc2}/2$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>$-V_{dc2}/2$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>$-V_{dc1}-(V_{dc2}/2)$</td>
</tr>
</tbody>
</table>

Fig. 2. Current flow through the switches of a leg on the four-level nested configuration.

Every switch is connected certain time only because in order to eliminate the short circuit through the leg. This nested multilevel inverter input voltages are selected as $V_{dc1}=V_{dc2}=V_{dc3}=V_{dc}$, which means that $V_{C1}=V_{C4}=V_{dc}$ and $V_{C2}=V_{C3}=V_{dc}/2$. 

Fig. 3. Current flow through the switches of a leg on the four-level NPC topology.
\[ V_1 = V_{dc1} + \frac{V_{dc2}}{2}, \quad V_2 = \frac{V_{dc2}}{2}, \quad V_3 = -\frac{V_{dc2}}{2}, \quad V_4 = -V_{dc3} - \frac{V_{dc2}}{2} \]

Fig. 2 shows the current flow directions (positive and negative currents) when the switches Sx1-Sx4 are turned ON, respectively. If Sx2, Sx3 are bidirectional controlled switches, this switches are employed in the inner leg and also Sx1,Sx4 switches are used in the outer leg. When positions of the switches (Sx1–Sx4) are changed, a short circuit was appear on the leg. Due to the reason is when outer leg’s switches are turned ON in the circuit.

III. PULSEWIDTH MODULATION (PWM) STRATEGY

The pulse width modulation is a technique which is characterized by the generation of constant amplitude by pulse duration by modulating the duty cycle. In the sinusoidal PWM technique we are having the modulated signal and the carrier signal if the carrier signal is to be of single then it is called single carrier based PWM technique. If the carrier signal is to be of multiple in order then it is called multi carrier based PWM control technique.

If this paper implemented by using the level shift pulse width modulation technique, there are phase disposition (PD), phase opposition disposition (POD) and alternative phase opposition disposition (APOD).

1. PHASE DISPOSITION

If phase disposition is defined as the all carriers are selected in the same phase, that is denote as phase disposition. It is used in this nested multilevel inverter, get the lowest total harmonic distortion, and also compared to the other modulation technics like as POD, APOD. The output waveforms of this method four, five & six levels are shown below.

![Fig.4. phase disposition of carrier wave](image)

![Fig.5. four level nested configuration three phase line to line pd output voltages](image)

![Fig.6. THD of four level phase disposition mode](image)
Fig. 7. Five level nested configuration three phase line to line pd output voltages

Fig. 8. THD of five level phase disposition mode

Fig. 9. Six level nested configuration three phase line to line pd output voltages

Fig. 10. THD of six level phase disposition mode
2. PHASE OPOSITION DISPOSITION

If the phase opposition disposition method (POD), all carrier signals are arrange the above the zero line reference voltage and below the line by 180 degrees as shown in below figure. if this phase opposition disposition technique was giving best harmonic results compare to the alternate phase opposition disposition. The output voltage waveforms of four, five & six levels are shown below.

Fig.11. phase opposition disposition of carrier wave

![Phase Opposition Disposition](image1)

Fig.12. four level nested configuration three phase line to line pod output voltages

![Four Level Output Voltages](image2)

Fig.13. THD of four level phase opposition disposition mode

![THD of Four Level](image3)

Fig.14. five level nested configuration three phase line to line pod output voltages

![Five Level Output Voltages](image4)
Fig. 15. THD of five level phase opposition disposition mode

Fig. 16. Six level nested configuration three phase line to line pod output voltages

Fig. 17. THD of six level phase opposition disposition mode

3. ALTERNATE PHASE OPPOSITION DISPOSITION

If the alternate phase opposition disposition method (APOD) is used to arrange the three carrier waves in disposition group, i.e., called as alternative phase opposition disposition. If all carrier signals are arranged above the zero line reference voltage and below the line by 180 degrees as shown in the below figure. This technique is similar to the phase opposition technique and also alternative phase opposition disposition technique was giving best harmonic results, but it was giving higher harmonics compared to the phase disposition and alternate phase opposition disposition. The output voltage waveforms of four, five & six levels are shown below.
Fig. 18. Apod carrier wave

Fig. 19. Four level nested configuration three-phase line-to-line apod output voltages

Fig. 20. THD of four level apod mode

Fig. 21. Five level nested configuration three-phase line-to-line apod output voltages
Fig. 22. THD of five level alternative phase opposition disposition mode

Fig. 23. THD of six level alternative phase opposition disposition mode

Fig. 24. THD of six level alternative phase opposition disposition mode

TABLE: 2. THD of four, five and six levels by using PD, POD and APOD techniques

<table>
<thead>
<tr>
<th>LEVEL</th>
<th>PD</th>
<th>POD</th>
<th>APOD</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>51.39</td>
<td>54.78</td>
<td>57.35</td>
</tr>
<tr>
<td>5</td>
<td>38.75</td>
<td>40.69</td>
<td>42.42</td>
</tr>
<tr>
<td>6</td>
<td>25.05</td>
<td>27.81</td>
<td>29.42</td>
</tr>
</tbody>
</table>
PMSM MOTOR

PMSM, it is a synchronous motor which the rotor windings are replaced by high resistivity permanent magnet material so no induced current in the rotor i.e. the rotor is lossless. In these motors (PMSM) the permanent magnet material is placed on the rotor by many methods. Among these methods, surface mounted magnets, inset magnets and buried magnet. Depending on these configurations, different properties of the machine are obtained. In case of surface mounted magnets, the rotor iron is approximately round and the stator inductance is low, as well as independent of the rotor position. The control of the machine becomes simple and the reluctance effect can be neglected. This paper also use permanent magnet synchronous motor, this pmsm motor is connect at the load and verify speed torque ripples.

Fig: speed of the pmsm
Fig: torque of the pmsm
Fig.25. four level speed torque ripples using pmsm

Fig: speed of the pmsm
Fig: torque of the pmsm
Fig.26. five level speed torque ripples using pmsm

Fig: speed of the pmsm
Fig: torque of the pmsm
Fig.27. five level speed torque ripples using pmsm
IV. CONCLUSION
This paper was completely involving the multilevel inverter based on the nested arrangement. This nested multilevel inverter is used to reduce the number of diodes compare to the neutral point clamping inverter and consequently get a higher efficiency. This paper was implemented by using level shift pwm techniques (PD,POD,APOD) to get the lower harmonics and also, the PMSM is to be fed with this nested multilevel inverter with different output voltage levels and performance comparison is to be accomplished in terms of torque ripples.

REFERENCES