Available Online at www.ijcsmc.com

International Journal of Computer Science and Mobile Computing

A Monthly Journal of Computer Science and Information Technology

ISSN 2320–088X

IJCSMC, Vol. 4, Issue. 12, December 2015, pg.282 – 288

Low Power Delay Product 10T Adder Circuit

MANOHARAN K, PUNITHA S

Assistant Professor, Department of Electronics and Communication Engineering, SVS College of Engineering, Coimbatore, India

Abstract: *In this paper, the various low power delay product full adder circuits have been analyzed. The adder is the fundamental blocks of any arithmetic circuit, so even a small reduction power or delay leads to improved performance of the circuit with optimal power saving. A 10T adder technique is the famous low power delay product full adder circuits with minimum transistor count. A new 10T technique based low power delay product full adder circuits have been proposed. To analyze the performance of proposed adder; the CMOS adder, 10T adder and proposed 10T adder are simulated using tanner EDA tools with 45nm technology. The power consumption in various sources and delay have been computed and analyzed for different supply voltage. Also power delay product and number of transistors for each design has been calculated and compared with other design. when VDD=1v, compared to Conventional CMOS the proposed 10T adder achieves power savings of 66.65%, PDP savings of 54.9% and area saving of 64% with the increased delay of 26%. It is also observed that compared to10T adder the proposed 10T adder achieves power savings of 36.11%, PDP savings of 50.69% and delay savings of 22.81%.*

Keywords: *Low power, Full Adder, 10T adder, Low Power delay products, Very Large Scale Integration Circuits*

1. INTRODUCTION

Nowadays portable device requires low power, high performance with lower area. The technology of battery life is not developed like integrated circuits. The battery cost of the device dominates the total cost of the product. The product cost can be reduced by extending the battery life via optimized power consumption without affecting performance. An adder is the fundamental circuit used for performing arithmetic operations. The total power of system can be extremely optimized by slightly reducing the power consumption in adder. Several researchers had designed low power, high speed adder with minimum number of transistors in static and dynamic logics. The function of a full adder is to add two binary numbers. It consists of three inputs a, b, c_{in} and two outputs sum and carry.

2. LITERATURE SURVEY OF FULL ADDERS

Conventional CMOS Full Adder [1] is the basic full adder designed using 28 transistors. In this adder, pull-down network was designed using NMOS transistors whereas pull-up network was designed using PMOS transistors. This adder provides stable output for all possible input combinations with higher noise margin. The leakage power consumption of the Conventional CMOS Full Adder is high. In the standby condition the leakage power contribute a crucial role in the total power consumption. Due to high transistor count the leakage power conception is more. Large number of PMOS transistor in the pull up network lead to high input capacitance which implies high delay and more power consumption.

Complementary pass transistor adder [2] was designed using NMOS pass transistor logic using 18 transistors. It provides low input capacitance so the high performance with low power is achieved. The power consumption is less compared to conventional CMOS full adder. In the output threshold loss occur due to NMOS transistors in the logic path. The noise margin of this adder is low it create problems in cascading the adder. The output must be computed for both direct and complement form. Transmission gate full adder [3] is similar to pass transistor logic instead of using NMOS; it is constructed using parallel combination of PMOS and NMOS. Due to the use of PMOS and NMOS transistors in parallel form no voltage degradation arises here. The

inputs are a, b and c and the outputs sum and carry. The problem with this adder is it requires double the transistor count and has lower driving capability.

The main benefit of using 10T full adders [4] is it consumes low power with minimum area. To produce full swing output using minimum transistor with low power consumption without affecting the performance is very hard. When designing a pass transistor logic based circuits the output voltage swing may be degraded by the threshold voltage. The lower output voltage swing may reduce the power consumption but the same time the noise margin of the circuit is getting reduced. Transmission function full adder [5] provides low power and has no power degradation but it has Lack of driver capability. 14T Full Adder [6] has good cascading capability, low power consumption and higher speed but requires more area. In Static Energy Recovery Full Adder [7] power consumption is reduced by using energy recovery technique but it does not provide full swing and it cannot be cascaded at low power supply voltage. 8T adder [8] provides low PDP but cascading fails at low voltage.

3. PROPOSED FULL ADDER

The stability of the circuit is affected due to the lower noise margin. The delay of the 10T full adder is high due to multiple stages in the circuit. A new 4T XOR gate has been proposed to overcome this problem. This gate provides high speed and low power consumption with minimum transistor count. The fig 1 shows the schematic diagram of XOR gate. When the input combination a=1 and b=0 the N1, P2 transistors are turned ON and N2, P1transistors are turned OFF. The output is logic 1 because the logic 1in the input a is connected to the output through P2 transistor. Similarly When the input combination a=0 and b=1 the N2, P1 transistors are turned ON and N1, P2 transistors are turned OFF. The output is logic 1 because the logic 1in the input b is connected to the output through P1 transistor. When the both the inputs are zero both PMOS transistors P1, P2 are turned ON and both PMOS transistors N1, N2 are turned OFF. The output is logic 0 because both transistor present in pull up network are turned ON now logic 0 in the input a is connected to the output through P2 transistor similarly logic 0 in the input b is connected to the output through P1 transistor. For these three input combinations pull up network is enough to get correct output. But the circuit with only pull up will fail for the input combination a=1 and b=1 because no discharge path available to get output logic as zero. This problem is solved by including pull down network of NMOS transistors in serious; this circuit will operate correctly for all the input combinations.

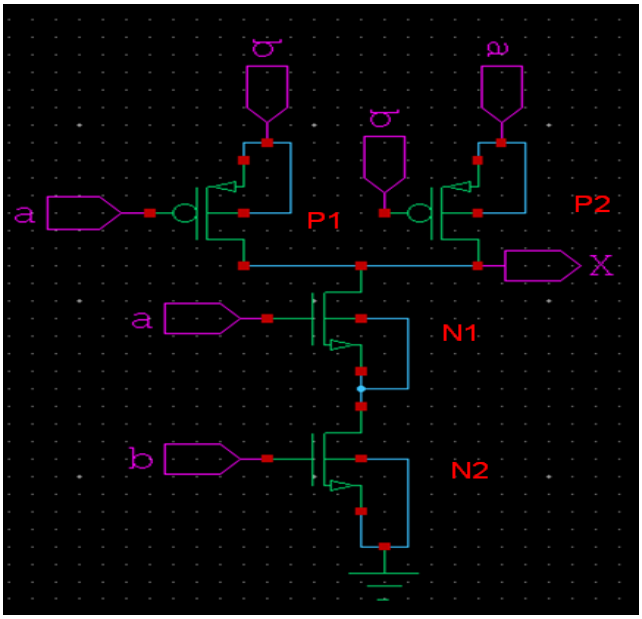

Figure 1: Proposed XOR gate.

By using the proposed XOR gate, a new 10T full adder is designed. The fig. 2 shows the schematic diagram of the proposed 10T full adder gate. The three single bit inputs a, b, cin are given to the circuit and the two outputs are sum and carry. The output of the full adder is based on following equation.

$$\text{Sum} = a \oplus b \oplus cin \quad (1)$$

$$\text{Carry} = a.b + cin\,(a \oplus b) \quad (2)$$

$$X = a'.\,b + a\,.\,b' \quad (3)$$

$$X = a \oplus b \quad (4)$$

Sum can be rewritten using half adder as

$$\text{Sum} = X \oplus cin = X'.\,cin + X\,.\,cin' \quad (5)$$

Carry can be rewritten using half adder as

$$\text{Carry} = a\,.\,X' + cin\,.\,X \quad (6)$$

=a . (a ⊕ b)' + cin . (a ⊕ b)
=a . (a.b + a'b')+ cin . (a ⊕ b)
= a.b + a.a'.b'+ cin . (a ⊕ b)
= a.b + 0 + cin . (a ⊕ b)
= a.b + cin . (a ⊕ b)

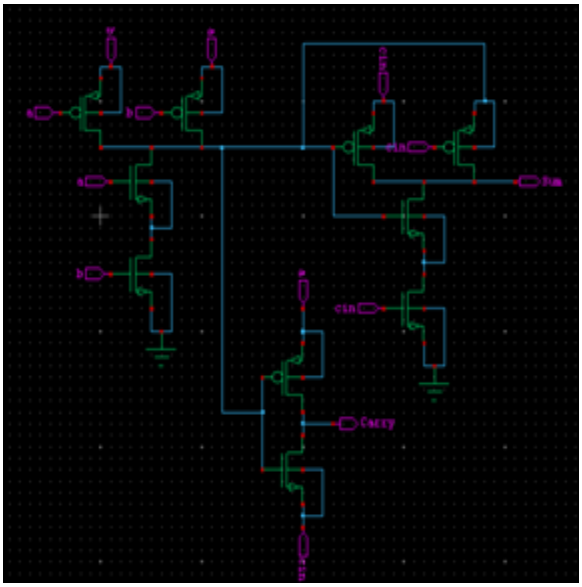

Figure 2: Proposed 10T Adder.

The output voltage waveform of proposed 10T adder for various input combinations are shown in fig. 3. From the output waveform the output sum and carry for different input combinations are verified with adder truth table.

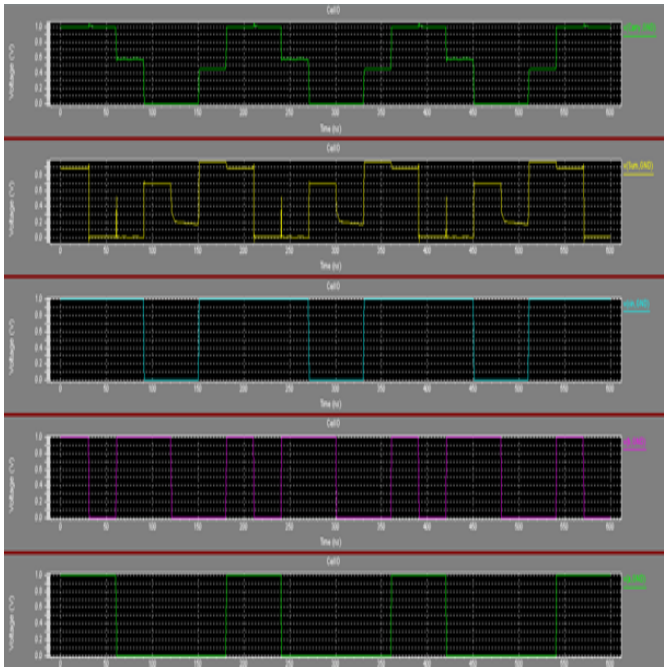

Figure 3: output voltage waveform of proposed 10T adder

4. RESULT AND DISCUSSIONS

To achieve low power and minimum delay proper W/L ratio for the proposed 10T adder is selected. The conventional CMOS, 10T adder and proposed 10T adder are simulated with the same input combinations and output logics sum and carry are verified. For the supply voltage Vdd=1V, the power dissipation in supply voltage VDD and input sources A, B, Cin and delay are measured for these adders and tabulated in table 1. Similarly the output logics for sum and carry also power and delay are calculated for supply voltage VDD=0.75V and VDD=0.5V tabulated in table 2 and table 3. The power is calculated as an average power of the circuit when operating at 50% switching activity. The total is calculated as summation of Supply voltage

power and all input power. The Propagation delay is calculated as the maximum delay between input crossing 50% of supply voltage to output crossing 50% of supply voltage. Power delay product (PDP) is calculated as product of delay and average power consumption. The powers are in the range of nano watts (nw), delays are in the range of Pico second (ps), and power delay products are in the range of auto joules (aj).

Table 1: Performance of adder at Vdd=1v.

Types	Power Dissipation (nW)					Delay (ps)	Power Delay Product (aj)
	Vdd	Input source A	Input source B	Input source Cin	Total		
CMOS Adder	2056	10.35	24.72	32.45	2123	126	267
10T Adder	774	0.36	17.71	5.57	1108	221	244
Proposed 10T Adder	0.00	237.85	235.17	235.17	708	170	120

From the table1 it is observed that when VDD=1v, compared to CCMOS the proposed 10T adder achieves power savings of 66.65%, PDP savings of 54.9% and area saving of 64% with the increased delay of 26%. It is also observed that when VDD=1v, compared to10T adder the proposed 10T adder achieves power savings of 36.11%, PDP savings of 50.69% and delay savings of 22.81%.

Table 2: Performance of adder at Vdd=0.75v.

Types	Power Dissipation (nW)					Delay (ps)	Power Delay Product (aj)
	Vdd	Input source A	Input source B	Input source Cin	Total		
CMOS Adder	1017	6.00	14.14	17.37	1054	230	243.20
10T Adder	319	0.54	52.11	13.15	449	422	190.17
Proposed 10T Adder	0.00	118.96	141.47	37.61	321	284	91.54

From the table 2 it is observed that when VDD=0.75v, compared to CCMOS the proposed 10T adder achieves power savings of 69.49%, PDP savings of 62.35% and area saving of 64% with the increased delay of 18.95%. It is also observed that when VDD=0.75v, compared to10T adder the proposed 10T adder achieves power savings of 28.43%, PDP savings of 51.86% and delay savings of 32.73%.

Table 3: Performance of adder at Vdd=0.5v.

Types	Power Dissipation (nW)					Delay (ps)	Power Delay Product (aj)
	Vdd	Input source A	Input source B	Input source Cin	Total		
CMOS Adder	227	2.36	6.01	9.20	244	360	88.18
10T Adder	82	0.35	27.93	7.69	118	520	61.65
Proposed 10T Adder	0.00	41.79	27.32	27.32	96	433	41.80

From the table 3 it is observed that when VDD=0.5v, compared to CCMOS the proposed 10T adder achieves power savings of 60.60%, PDP savings of 52.35% and area saving of 64% with the increased delay of 16.88%. It is also observed that when VDD=0.5v, compared to10T adder the proposed 10T adder achieves power savings of 18.65%, PDP savings of 32.2% and delay savings of 16.65%.

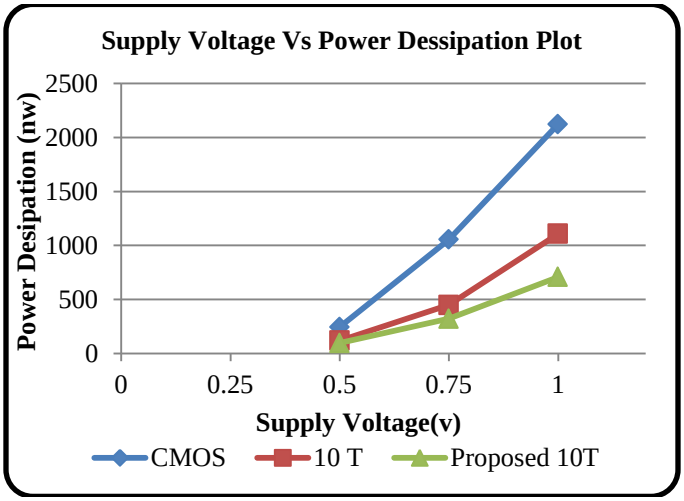

Figure 4: Supply Voltage Vs Power Dissipation Plot

The fig.4 shows plots of supply voltage verses Power dissipation of CMOS adder, 10T adder and proposed 10T adder for supply voltages Vdd=1v, Vdd=0.75v and Vdd=0.5v.
It is observed from the fig that the reduction of supply voltage VDD will abruptly decrease the average power consumption of the circuit.

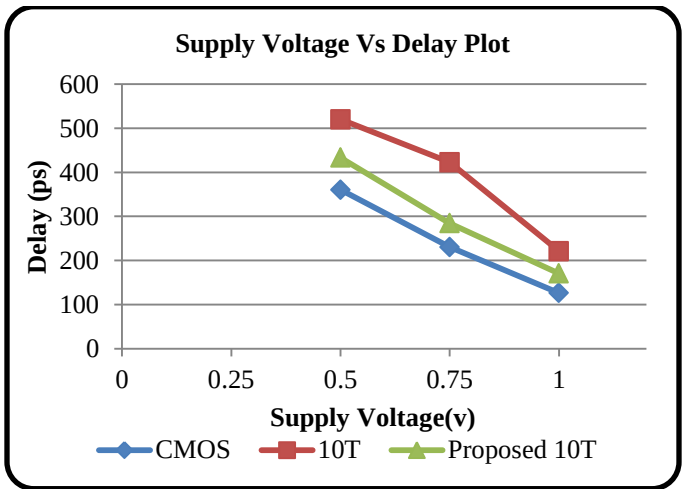

Figure 5: Supply Voltage Vs Delay Plot

Fig. 5 shows plots of supply voltage verses delay of CMOS adder, 10T adder and proposed 10T adder for supply voltages Vdd=1v, Vdd=0.75v and Vdd=0.5v. It is observed from the fig that the reduction of supply voltage VDD will increase the propagation delay of the circuit. Due to the increase in the delay, the operating speed performance of the adder is getting reduced.

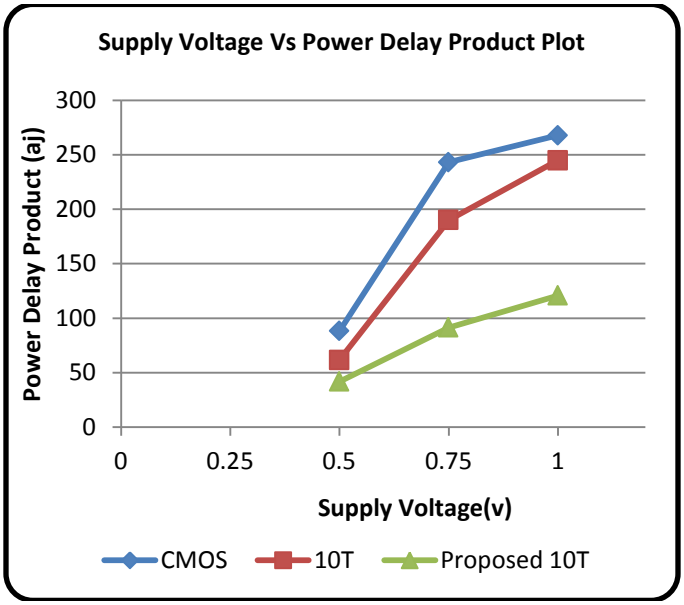

Figure 6: Supply Voltage Vs Power Delay Product Plot

The fig 6 shows plots of supply voltage verses Power delay product of CMOS adder, 10T adder and proposed 10T adder for supply voltages Vdd=1v, Vdd=0.75v and Vdd=0.5v. It is observed from the fig that the reduction of supply voltage VDD will decrease the propagation delay of the circuit. It results the operating speed performance of the adder is get reduced.

Table 4: Transistor count for different adder configuration

Adder configuration	Number of transistors used
CMOS Adder	28
10T Adder	10
Proposed 10T Adder	10

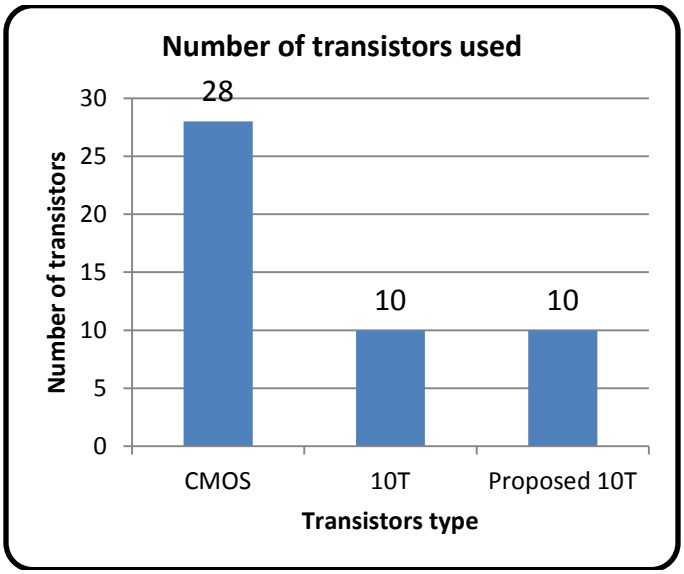

Figure 7: Number of transistors used in the design

5. CONCLUSION

The proposed 10T based low power delay product full adder circuit is simulated using tanner EDA tools with 45nm technology. The simulation is carried out for different supply voltage and the results like power consumption in various sources, delay, power delay product are tabulated. Similarly CMOS adder and existing 10T adder also simulated different supply voltage and the results are tabulated. Also no of transistor used for different design has been tabulated. when VDD=1v, compared to Conventional CMOS the proposed 10T adder achieves power savings of 66.65%, PDP savings of 54.9% and area saving of 64%

with the increased delay of 26%. It is also observed that compared to10T adder the proposed 10T adder achieves power savings of 36.11%, PDP savings of 50.69% and delay savings of 22.81%.

REFERENCES

[1] N.H.E. Weste and K. Eshraghian, Principles of CMOS VLSI design: A System Perspective, Reading, Massachusetts: Addison Wesley, 1993.

[2] R. Zimmermann, and W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," IEEE J. Solid State Circuits, vol. 32, no. 7, pp. 1079-1090, Jul. 1997.

[3] M. H. Moaiyeri, R. F. Mirzaee and K. Navi, "High Speed NP-CMOS and Multi-output Dynamic Full Adder Cells", International Journal of Electrical and Electronics Engineering, Volume 4, Issue 4, 2010.

[4] K. Navi, M. Maeen, V. Foroutan, S. Timarchi, and O. Kavehei, " A Novel low-power Full Adder cell for low voltage", Integration, the VLSI Journal, Volume 42,issue 4, 2009.

[5] Nan Zhuang and Haomin Wu, "A new design of the CMOS full adder" IEEE Journal of Solid State Circuits, Vol. 27, No.5, pp. 840-844, May 1992.

[6] Dr. P.T. Vanathi, Dr. J. Ramesh,K. Revathy, R. Preethi, C. Haritha Laxmi and K. Keerthan, "Performance Analysis of High Performance Adder Architectures" ,Volume 2, Issue 1, 2012

[7] R. Shalem, E. John, and L. K. John, "A novel low-power energy recovery full adder cell," in *Proc. Great Lakes Symp. VLSI*, Feb. 1999, pp. 380–383.

[8] A. Bazzazi, A. Mahini and J. Jelini "Low Power Full Adder Using 8T Structure" Proceeding of IMECS Volume-II, Hong kong., March 2012.

