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RESEARCH ARTICLE

DESIGN AND IMPLEMENTATION OF INTELLIGENT TRAFFIC LIGHT SYSTEM

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ABSTRACT: ***Traffic lights are the signaling devices used to manage traffic on multi-way road. These are positioned to control the competing flow of the traffic at the road intersections to avoid collisions. By displaying lights (red, yellow and green), they alternate the way of multi-road users. The implementation of traffic Light Controller can be through a Microcontroller, Field Programmable Gate Array or Application Specific Integrated Circuit. FPGA implementation is advantageous over ASIC and microcontroller; number of IO ports and performance compared to microcontroller and implementation with FPGA is less expensive compared to ASIC design. This paper presents the FPGA implemented low cost advanced TLC system using ChipScope Pro and Virtual Input Output. The TLC implemented is one of the real and complex signaling lights in Kingdom of Bahrain, for pedestrian way included four roads and sensors and camera assisted motorway.***

Index Terms—ChipScope Pro, Virtual Input Output, Integrated Controller, Field Programmable Gate Array.

I. INTRODUCTION

FPGA is an Integrated Circuit consisting of an array of uncommitted elements; interconnection between these elements is user-programmable. Using Random Access Memory, high density logic is provided. FPGA is advantageous compared to microcontroller in terms of number of IO (input & output) ports and performance. FPGA, an inexpensive solution compared to ASIC design; is effective with respect to cost in the case of production of large number of units but for fabrication in small number of units it is always costly and time consuming. The Design flow of FPGA shown in Fig. 1 is used to implement the traffic light controller using FPGA. The circuit description can be done using HDLs, followed by the functional simulation and synthesis. The design flow is followed till the timing simulation and then the generated file is downloaded into the target device (FPGA). Verilog is used as HDL for circuit description to code the TLC module. Verilog HDL is used because of the difficulty in writing a VHDL code which has to integrate the source code, ChipScope Pro-Integrated Controller (ICON) and Virtual Input Output (VIO).

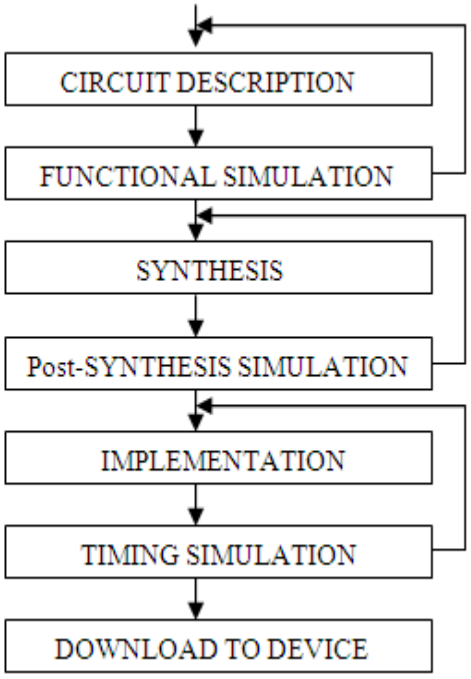

Fig. 1 FPGA Design Flow

At first the North traffic will be allowed to move and then traffic in the East, South and West direction will be allowed to move in sequence. The advantage of writing Traffic Light Controller program is that in a program, modifications as per requirements can be done easily i.e., suppose the traffic on main road should be allowed for more time and for side roads the traffic should be allowed for less time; then the clock is divided in such a way that for main road the clock period will be more and for side roads the clock period will be less, this is because the main road traffic is heavy when compared to the side road traffic [5]. In general TLC System will be having three lights (red, green and yellow) in each direction where red light stands for traffic to be stopped, green light stands for traffic to be allowed and yellow light stands for traffic is going to be stopped in few seconds. But in this paper, yellowlight is split into two phases and are included in the signaling lights along with red and green lights in order to indicate that in the first phase of yellow light, pedestrian wille OFF and in the second phase, pedestrian will be ON. Traffic congestion has been causing many critical problems and challenges in most cities of modern countries. To a commuter or traveler, congestion means lost time, missed opportunities, and frustration. To an employer, congestion means lost worker productivity; trade opportunities, delivery delays, and increased costs. To solve congestion problems is feasible not only by physically constructing new facilities and policies but also by building information technology transportation management systems.

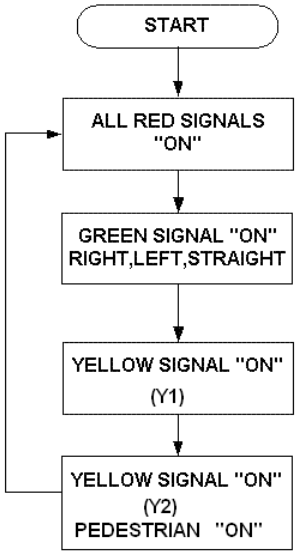

Fig. 2 TLC Flow Chart

The sequential order of the flow chart helps the programmer in the design regarding the flow of the program. North/ south-bound traffic will start with a green signal light while all the other lanes being red, the traffic will be stopped. After a predetermined time, the north/south traffic light turns yellow and then to red, allowing the east/west signal light to be green and the same sequence as the north/south-bound traffic is followed. The system will continue to be in this loop until an indication of a vehicle in a left turn lane occurs. When the signal light turns yellow, the controller scans the inputs. If high, then the program will jump to a subroutine which has a different light sequence. This sequence controls the main lights along with the left turn lights. After completion of the subroutine sequence, the program returns to the main loop. The flow chart can be applied to any number of road structures. In this paper, a four road structure is considered in which the four directions labeled with four labels namely North, South, East and West. Each traffic lane has set of three traffic light signals, "Red, Yellow, and Green", which operates similar to genera signaling lights i.e., it changes from red to green and then to yellow and after that back to red signal.

II. STRUCTURE OF ROAD

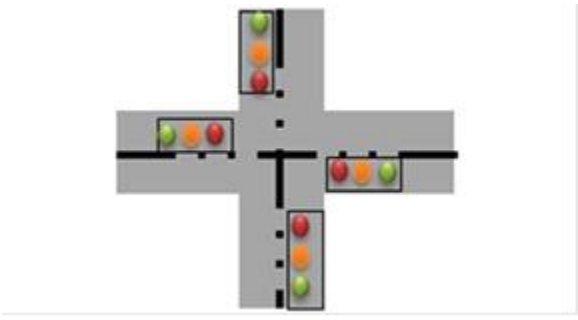

Fig. 3 A Single junction of Four Roads

In the conventional traffic light system there are four LEDs used on each sides in order to reduce the power consumption we make use of motor and reduce the number of LEDs to five as shown in fig.2.

In the above structure we use five LEDs which is three red LEDs and each yellow and green LEDs. All the red LEDs will always remain on and yellow , green LEDs turn on with The sequential order of the flow chart helps the programmer in the design regarding the flow of the program. North/ south-bound traffic will start with a green signal light while all the other lanes being red, the traffic will be stopped. After a predetermined time, the north/south traffic light turns yellow and then to red, allowing the east/west signal light to be green and the same sequence as the north/south-bound traffic is followed. The system will continue to be in this loop until an indication of a vehicle in a left turn lane occurs. When the signal light turns yellow, the controller scans the inputs. If high, then the program will jump to a subroutine which has a different light sequence. This sequence controls the main lights along with the left turn lights. After completion of the subroutine sequence, the program returns to the main loop. The flow chart can be applied to any number of road structures. In this paper, a four road structure is considered in which the four directions labeled with four labels namely North, South, East and West. Each traffic lane has set of three traffic light signals, "Red, Yellow, and Green", which operates similar to genera signaling lights i.e., it changes from red to green and then to yellow and after that back to red signal.
The motor will rotate every time after the yellow LED.
In the fig. 2.(a) it is shown that the there is one LED in the North South direction which is red and fig.2.(b) there is one LED in west direction which is red and two LEDs in east direction which are green and yellow. The green LED will remain on and after that yellow then the motor will rotate 90' to the south direction and again the green will on and the red LED of the north direction will move to the east direction and hence the rotation continue through whole cycle. Finite state machine has been used to control the traffic lights at the intersection of a north-south and an east-west route. Initially all RED signals are ON and after few seconds, GREEN of a signal light in one particular direction will be ON to allow the traffic in straight, right and left paths[5-7].
Firstly the traffic of the North side will be allowed to move and then traffic in the East, South and West direction will be allowed to move in sequence. The PTLC program will allow to do modification as per requirements i.e. the clock is divided in such a way that the clock period can be increased or decreased as per the load of traffic on the road. The road with heavy traffic will be allowed a more clock period than a road with a low traffic[8]. The conventional TLC System will be using three LED's (red,green,yellow) in each direction where Red LED stands for traffic to be stopped, Green LED stands for traffic to be allowed and Yellow LED stands for traffic is going to stopped in few seconds. But this paper contain a motor which will rotate after the yellow signaling. North bound traffic will start with a green signal light while all others being red ,the traffic will be stopped. After a predetermined time, the north light will become yellow and then motor rotates it will turns red, allowing the east to be green and same sequence as north bound traffic is followed. The system will continue in this loop.

III. STATE MACHINE, STATE TABLE AND HARDWARE DESCRIPTION

The TLC state diagram shown in Fig. 3 illustrates that whenever cnt=00 and dir=00,then green light in north direction will be ON for few seconds and red signal light in all other directions namely west, south and east will be ON. When cnt=01 and dir=00 then yellow light (y1) will be ON for few seconds and when cnt=01 yellow light (y2) and pedestrian north will be ON and then dir is incremented by one and cnt is assigned to zero. So when cnt=00 and dir=01, the green light in east direction will be ON for few seconds and all red lights in other directions be ON.

A finite state machine (FSM) is a mathematical model of computation used to design the sequential logic circuits. The machine is in only one state at a time, the state it is in at any given time is called the current state. It can change from one

state to another when initiated by a triggering event or condition, this is called transition.The output is produced by the system in order to the response of the input signal frominput handling module [9-10].

In this design, PTLC uses a standard two process finite state machine where one process is used to change states of every clock cycle while the other process is used to combinatorial calculate what the next state should be based on the current inputs and the current state.

Table I. Terms used in State Diagram

South	West
GS= green south RS= right south Y1S=yellow light1south Y2S= yellow light 2 south PDS=pedestrain south	GW = green west RW = right west Y1W = yellow light 2 west Y2W = yellow light 2 west PDW = pedestrain west
North	**East**
GN = green north RN = red north Y1N = yelow light 1 east Y2N = yellow light 2 north PDN = pedestrain north	GE = green east RE = red east Y1E = yellow light 2 east Y2E = yellow light 2 east PDE = pedestrain east

Whenever cnt=01 and dir=01 then yellow light (y1) will be ON for few seconds and when cnt=01 yellow light (y2) and pedestrian east will be ON and then dir is incremented by one and cnt is assigned to zero. So whenever cnt=00 and dir=10, the green light in south direction will be ON for few seconds and all red lights in other directions will be ON. Whenever cnt=01 and dir=10 then yellow light (y1) will be ON for few seconds and when cnt=01 yellow light (y2) and pedestrian south will be ON and then dir is incremented by one and cnt is assigned to zero. So whenever cnt=00 and dir=11, the green light in west direction will be ON for few seconds and all red lights in other directions will be ON. Whenever cnt=01 and dir=11 then yellow light (y1) will be ON for few seconds and when cnt=01 yellow light (y2) and pedestrian west will be ON and then dir is assigned to 00 and cnt is assigned to zero. This sequence repeats and the traffic flow will be controlled by assigning time periods in all the four directions. Table I specifies the abbreviations used in TLC state diagram. Labeling for each lane is done by assigning the

direction label in order to distinguish the outputs from each other with their states. In the traffic light controller program there will be two inputs namely clock and reset. When the two variables are „1" then the TLC will start working. Initially that is when reset is „0" then the red signal lights in all the directions will be ON and when reset is „1", then the traffic light controller system will be on assigning cnt and dir variables to 00 where cnt and dir respectively represent the states and the four directions in the state machine.

IV. RESULTS

4.1 RTL SCHEMATIC:

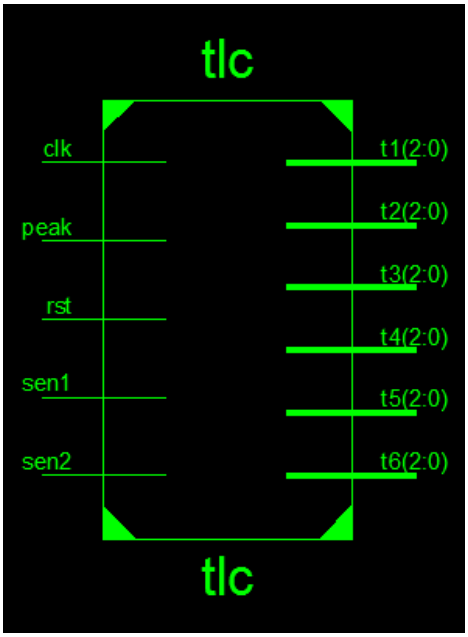

Fig. 4 RTL Schematic

The synthesis is performed by Xilinx 12.4. The RTL schematic shown above is a proposed tlc. It consists of two input signals, clock signal, reset signal and stages.

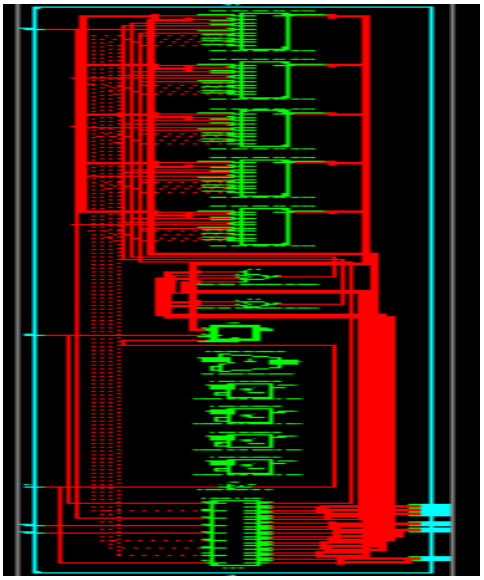

Fig. 5 RTL Schematics with 5 Counters, Adder, D Flip-flop, 4 Comparators, Inverter, FSM

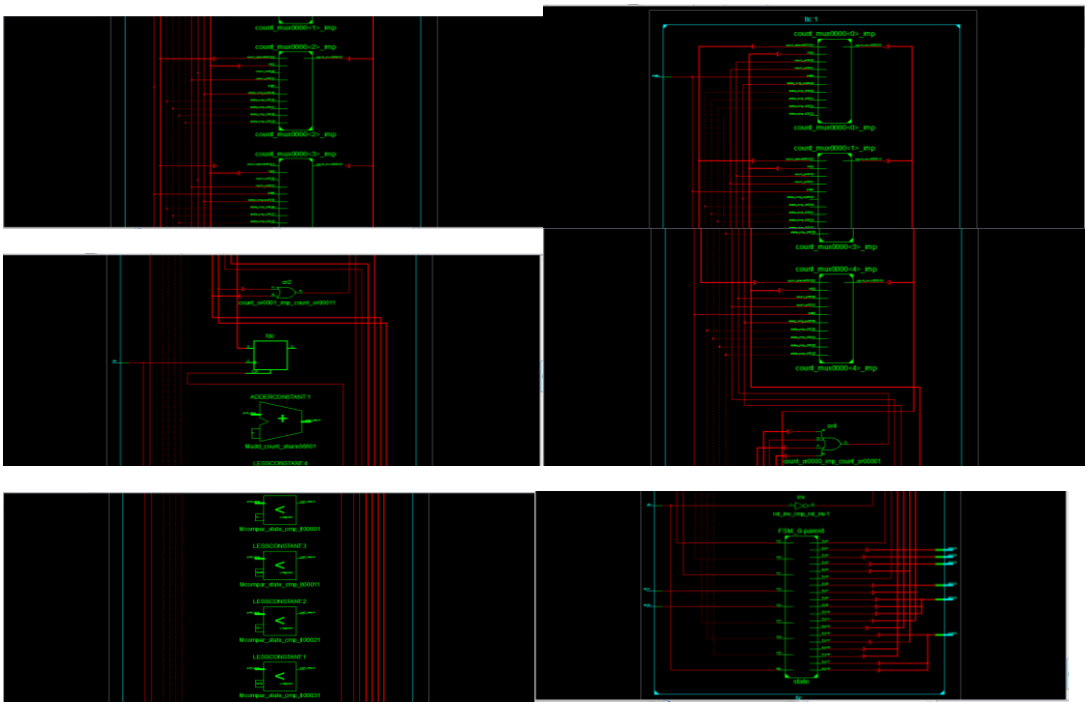

Fig. 6 RTL Schematics zoom in

4.2 SIMULATION RESULTS:

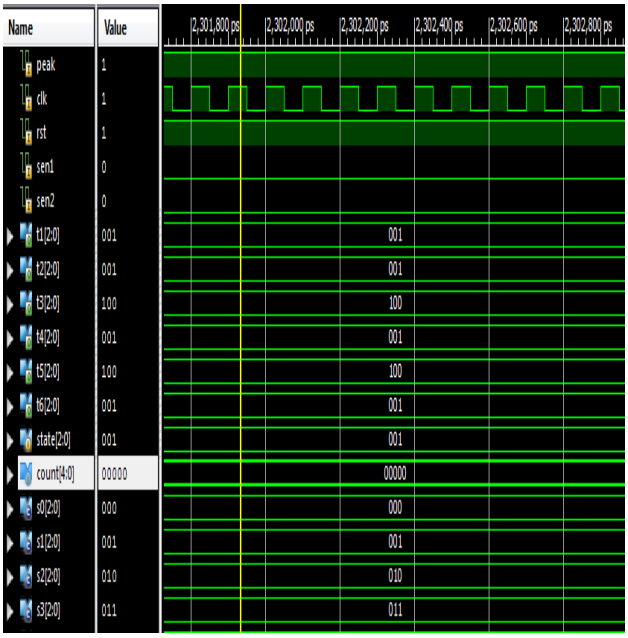

Fig.7 Sensor1=0, Sensor2=0

The simualtion results are carried out by using modelsim 6.4b . Here two inputs are indicated with Sensor1=0, Sensor2=0. and out put is indicated with R. When the clock signal is '1' and reset signal is '0' the output will be displayed.

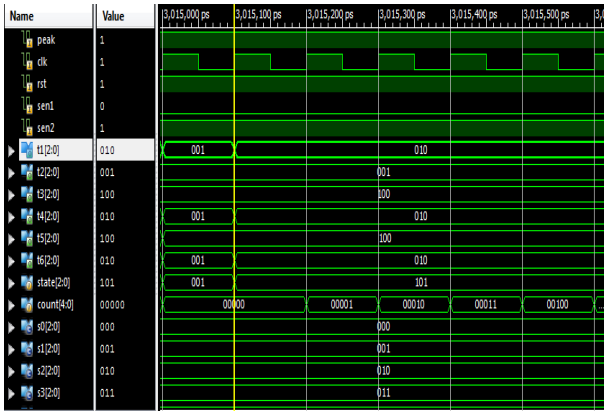

Fig. 8 Sensor1=0, Sensor2=1

The simualtion results are carried out by using modelsim 6.4b . Here two inputs are indicated with Sensor1=0, Sensor2=1. and out put is indicated with R. When the clock signal is '1' and reset signal is '0' the output will be displayed.

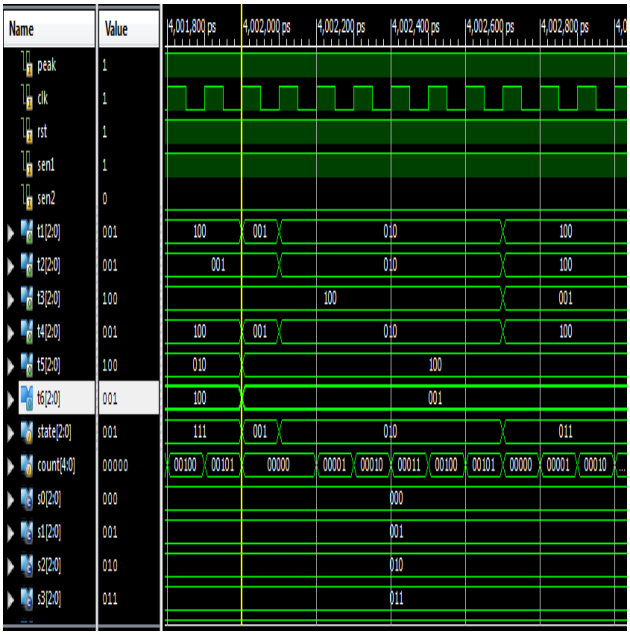

Fig. 9 Sensor1=1, Sensor2=0

The simualtion results are carried out by using modelsim 6.4b . Here two inputs are indicated with Sensor1=1, Sensor2=1. and out put is indicated with R. When the clock signal is '1' and reset signal is '0' the output will be displayed.

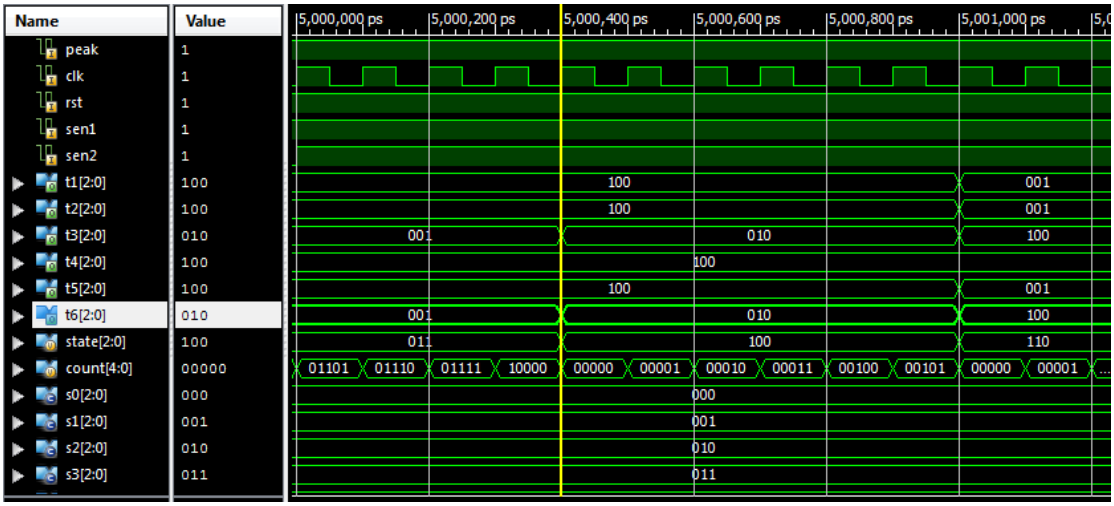

Fig. 10 Sensor1=1, Sensor2=1

The simualtion results are carried out by using modelsim 6.4b . Here two inputs are indicated with Sensor1=1, Sensor2=1. and out put is indicated with R. When the clock signal is '1' and reset signal is '0' the output will be displayed.

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