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RESEARCH ARTICLE

FGPA Implementation of High Speed 16 – Bits Vedic Multiplier using LFSR

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Abstract- This paper describes the implementation of a 16-bit Vedic multiplier enhanced in terms of propagation delay and automatic insertion of all possible combinations of inputs. In our design the architecture is consist of PID and BSM along with LFSR. The design is implemented and verified using FPGA and ISE Simulator. The core was implemented on Xilinx Spartan-6 family xc6s1x75T-3-fgg676 FPGA. The propagation delay comparison was extracted from the synthesis report and static timing report as well. Linear Feedback Shift Register has been used to automate the insertion of all possible combination of 16×16 bits. This will make this project compatible with testing devices. The minimum period is reduced to 4.872ns at Maximum Frequency of 205.255MHz.

Key Words: PID, BSM, LFSR, Propagation Delay

1. Introduction

Any technology which basically do arithmetic functioning uses computational unit. Multiplication is the one of the four pillar of arithmetical manoeuvres. Scientists and engineers persistently searching for new algorithms and hardware for the employment of this methodology.

In cryptology (encryption and decryption) or digital signal processing and even other logical computations a Multiplier is essential most hardware blocks to apply such procedures. Designing of Faster, better and uses less strengths, minimal in magnitude multiplier is a relentless battle, numerous researcher are in belvedere to construct such multiplier.

In Standard DSP the multiplier is a crucial component, a general working of a DSP necessitate numerous multiplications dynamically, and this arithmetic operation has wide uses for DSP.

As one may know Mathematics is the core science's universe. The Indian developed many sutras perform mathematical operations, the Indian System for mathematical functioning was since know as Vedic Mathematics, which was much more simpler and easier to accomplish than any conservative mathematics ever developed.

Conservative mathematic techniques generate a large quantity of delay in the employment of system, in multiplier of N-bits, which spontaneously brings diminution in execution. Whereas the Vedic maths has proven too that it's augmented above all of this, and no such delay transpires, a go to technique to execute arithmetic manoeuvre.

The Vedic mathematics is entailed of sixteen Sutras, which fetches accuracy in calculations and make it swifter. This technique solves problems dealing with hefty numbers in minimal period quantum, work completely differently from other strategies.
In dissimilarity to conventional methods the Vedic mathematics is stronger and faster technique to perform calculative operations as the conventional methods produce quantitative delays in implementation of n – bit multiplier hardware resulting in combination of delay and diminution of enactment. The architecture selection criteria of FPGA or ASIC is support system for hardware grounded multiplication.

2. Vedic Sutras

Veda is verbatim for Vedic, which accurately means inventory of all knowledge, it contains sixteen Sutras which is associated with numerous branches of Mathematics such as algebra, arithmetic or geometry etc.
Vedic Sutras is applied on and for every sector of Mathematics including solving complicated issues containing quantitative nos. where mathematical functions is done, which extremely save period quantum and efforts applied during the elucidation of numerical issues in comparison with other conventional methods present in the trend.
Book of Wisdom called Vedas is categorized in four dimensions, the proposed work for Vedic mathematics is an arm of Sthapatya Veda, constructed on civil engineering and architectureanUpa – Veda (enhancement) of Atharva Veda, which explain many mathematic terminology such as arithmetic geometry. Quadratic equations, factorization, calculus, and trigonometry etc.
The embracement of all 16 mathematical formulae is called Vedic Mathematics, which ultimately form Vedas.

The proposed Vedic multiplier used changed version of Urdhva-tiryagbhyam Sutra and of Nikhilam Navatascaramam Dasatah which amplify the performance of multiplier in comparison with any other kind of conservative multiplier, which is instigated using FGPA in today's generation.

3. Proposed Multiplier Architecture Design

Assume there are two 16-bit numbers to be multiplied. Let it be X and Y which are the multiplier and multiplicand respectively.
Though the number designation is different but the implementation of architecture may same to some extent to evaluate the numbers.
The mathematical countenance for revised Nikhilam Sutra is specified beneath.

P=X*Y=(2^k2)*(X±Z2*2^(k1-k2))±Z1*Z2.– (1)

Where k1, k2 are the supreme power index of input numbers X and Y correspondingly. Z1 and Z2 are the remainders in the nos. X and Y correspondingly. [2]
The hardware deployment with automatic insertion of inputs X and Y partitioned into five blocks

A. Linear Feedback Shift Register
B. Base Selection Module
C. Power Index Determinant Module
D. Multiplier
E. Comparator

4. Implementation of Functional Blocks in Proposed Design

A. Linear Feedback Shift Register

A shift register whom contribution (known as input bit) is a linear function of aforementioned state. The most ordinarily expended LF of singular bit is exclusive – or, therefore LFSR also uses it for input. Seed is preliminary denomination for LFSR Probable states of few nos. are predetermined for the registers, thus it ultimately arrives in reiterating cycle.
LFSR can harvest an arrangement of bits that give the impression of being randomly chosen, and has a very elongated cycle if provided an adequately selected feedback function. Pseudo random nos. /noises, arrangement could be engendered with the solicitation of LFSRs, as well as fast digital counters, and blanching arrangement. Both the H/W and S/W deployment of LFSR is equivalent.

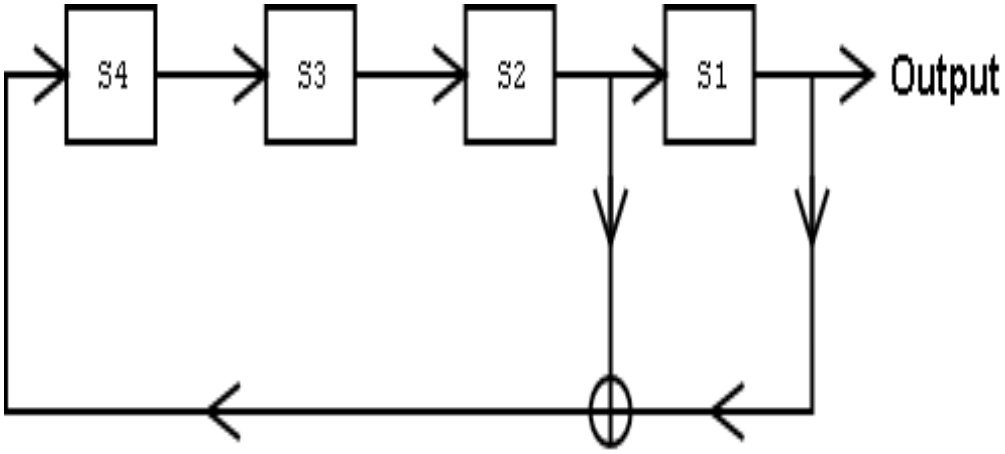

Fig. 3.1: Linear Feedback Shift Register (LFSR)

B. Base Selection Module

PIS as sub – module is included with Base selection module, beside the barrel shifter, comparator, multiplier, average determinant and an adder.

Operation:

An input of16-bit number is fed to power index determinant (PID) for interpretation of its maximum power which is fed to barrel shifter and adder.

The adder output/inputs leaned to shifter is correspondent with output of barrel shifter ('n' no. shifts) Multiplexer acquires the outputs from barrel shifter and with comparator input as an assortment line.
Comparator is foraged outputs of mediocre determinants and barrel shifter. In the harmony between multiplexer inputs and respective assortment line the required base is acquired.

C. Power Index Determinant Module

The shifting of input bits is done after an input no. is served to a shifter, by 1clock cycle.
To pursue if or not the no. is shifted or did not, by assignment of a sifter pin. In PID sequential assortment is deployed to explore from 1^{st} one in I/P no. originated from most significant bit.
Counter denomination will be decremented until I/P search bit is 'One' if the examined bit is founded to be 'Zero' Power index of I/P no. is requisite for O/P of the decrementer.

D. Multiplier Architecture

B.S.M. and P.I.D. is dominating section of M.A. With the help of barrel shifter the structural unit analyses the mathematical exhibit in the eq.
Base is assimilated by foraging 2 input nos. to the Base selection module, thus the base is acquired, the O/P of BSM and I/P nos. are foraged to the subtractor. Left over parts of z1 and z2 are assimilated by subtractor block BSM help sending required I/Ps to the PID of corresponding I/P nos.
Subtractor calculates the denomination whereas the A subsection of P.I.D. is exercised to acquire the power of base. These O/Ps obtained by the subtractor are foraged to the Multiplier that eats I/P of 2^{nd} adder/subtractor. Similarly PID's O/P are foraged to the 3^{rd} sub. Which eats on the I/O of the barrel shifter. The O/P of 2^{nd} Barrel shifter is acquired by, solicitation of I/P no. x and O/P of Barrel shifter are abridged to 1^{st} adder/subs. Thus it an transitional value is attained. Finally 2^{nd} adder/subs. will be the sub – section of planned M.A. which will give us the prerequisite response.

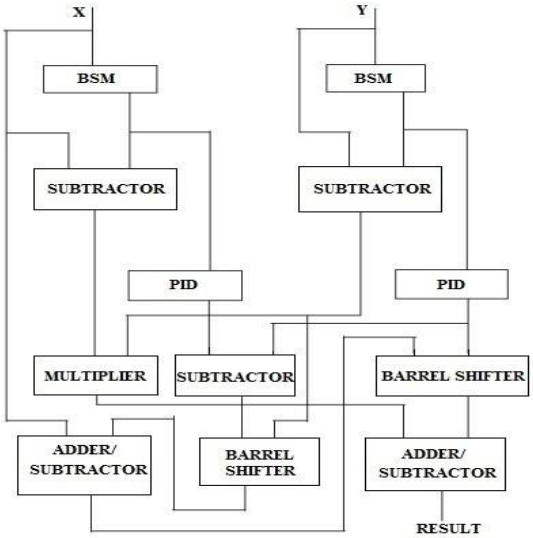

Fig. 3.4 Multiplier Architecture [2]

E. Comparator

Comparator is a habitual compositional logic circuit maneuverer in this planned architecture design.
As its name signifying this logical unit associate between two entities which are its input fed to it. Here the two inputs fed to it are the output if both the multipliers namely the conventional array multiplier and the planned Vedic multiplier architecture.
The basic function of this comparator here is to compare the output obtained from both the multipliers which are the conventional array multiplier and the proposed Vedic multiplier architecture. And to reflect whether both the given inputs to the comparator are equal or not by generating logic '0' or logic '1'.

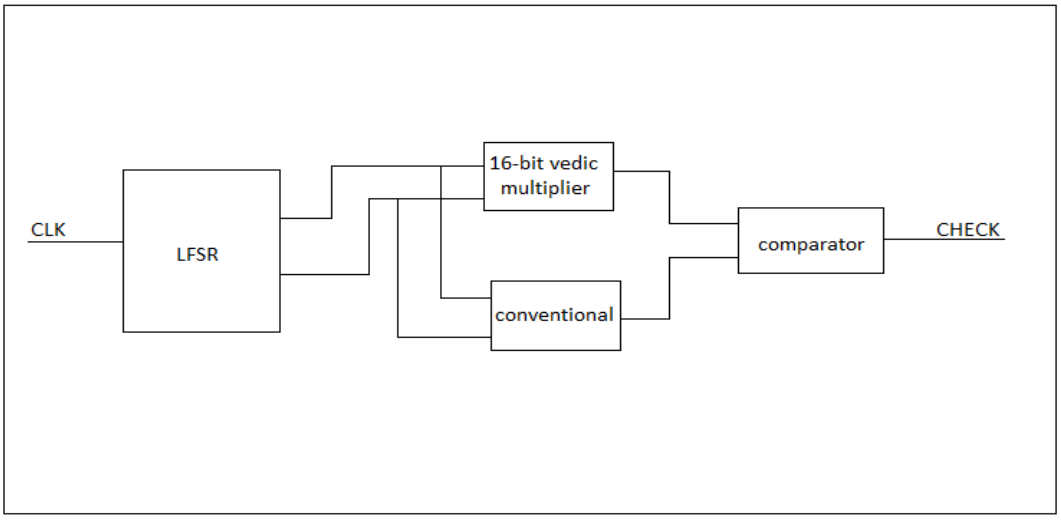

Fig. 3.3 Block Diagram of Proposed Architecture.

4. Result and Simulation Synthesis Proposed work

The work done in this paper opted for the result given below. The simulation synthesis and comparative quantities are also given as follow. The RTL obtained is as follow**.**

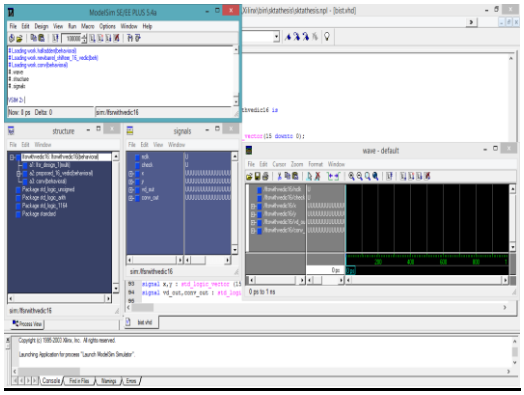

Fig. 4.5 Post Route Simulation

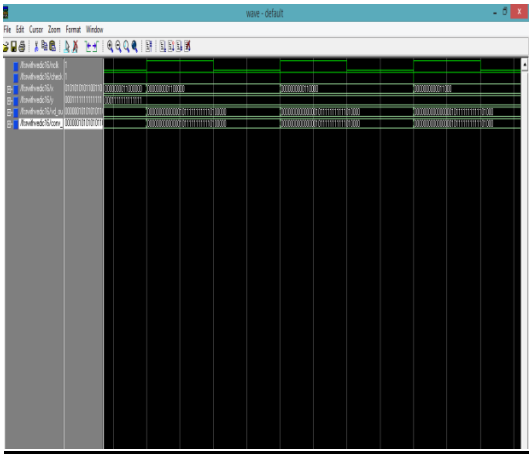

Fig. 4.6 Comparison Output Wave Of conventional and Proposed Vedic Multiplier

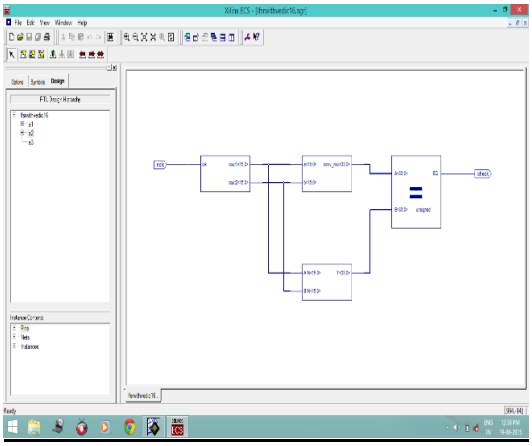

Fig. 4.7 RTL View Of 16-bit Vedic Multiplier Using LFSR

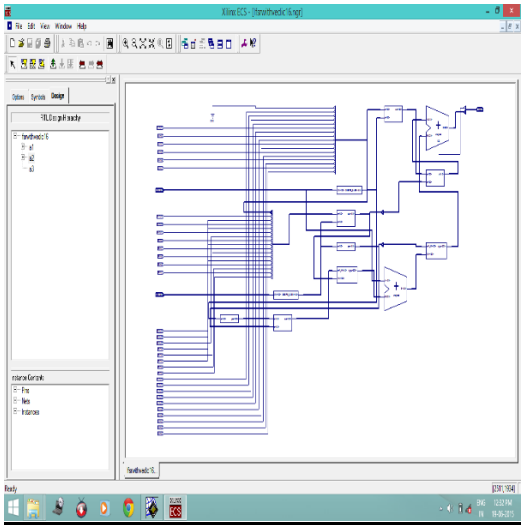

Fig. 4.9 RTL View of Proposed Vedic Multiplier

Comparative Table between Various Vedic Multiplier

Parameter	**Conventional Vedic Multiplier**	**8-bit Vedic Multiplier Proposed by A.Radhika in 2014[2]**	**16-bit Optimized Vedic Multiplier By G.Ganesh Kumar in 2012[3]**	**Proposed 16-bit Vedic Multiplier Using LFSR**
Delay (ns)	**43.42**	**6.781**	**31.526**	**4.872**

5. Conclusion

In this project a new technical approach has been proposed for multiplication using Vedic Mathematical technique. The delay of FPGA Implementation of high speed 8-bit Vedic multiplier using barrel shifter by Miss. A. Radhika, 978-1-4673-6150-7/13/$31.00 ©2013 IEEE has been reduced and implemented to 16-bit rather than 8-bit. The work is done on 16-bits and associated with Linear Feedback Shift Register.

Linear Feedback Shift Register has been used to automate the insertion of all possible combination of 16×16 bits. This will make this project compatible with testing devices. The minimum period is reduced to 4.872ns at Maximum Frequency of 205.255MHz.

The speedy and automatic implementation of inputs make this project applicable with various digital electronics applications such as image processing and etc. In future this work can be associated with different Vedic technique and can increase its area of application.

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