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RESEARCH ARTICLE

Architecture of Discrete Wavelet Transform Processor for Image Compression

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Abstract— Image compression is one of the major image processing techniques. Discrete wavelet transforms is the most popular transformation technique adopted for image compression. This paper presents an efficient VLSI architecture of a high speed, low power 2-D Discrete Wavelet Transform computing. There are number of architectures are present for realizing DWT. Based on the application and the constraints imposed, the appropriate architecture can be chosen. Proposed DWT architecture uses Harr transformation. In this architecture we will use parallel and pipelined processing logic. As we are using parallel and pipelined scheme it will provide fast computation of DWT. Thus, it is very suitable for new generation image compression systems, such as JPEG2000.

Key Terms: - Discrete Wavelet Transforms (DWT); JPEG2000; 2D-DWT; VLSI architecture; FPGA implementation

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