Available Online at www.ijcsmc.com

International Journal of Computer Science and Mobile Computing

A Monthly Journal of Computer Science and Information Technology

ISSN 2320–088X

IJCSMC, Vol. 3, Issue. 11, November 2014, pg.746 – 750

RESEARCH ARTICLE

High Speed OFDM Implementation in FPGA

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Abstract— FPGA is one of the efficient & economic way to implement the circuit. Orthogonal Frequency Division Multiplexing (OFDM) is a multicarrier modulation technique. OFDM provides high bandwidth efficiency because the carriers are orthogonal to each other and multiple carriers share the data among themselves. The main advantage of this transmission technique is their robustness to channel fading in wireless communication environment. This paper illustrates how QAM modulation scheme give higher speed in implementing OFDM in FPGA.

Keywords—FPGA (Field Programmable Gate Arrays); Orthogonal frequency division multiplexing (OFDM); Field programmable gate array (FPGA); Hardware description language (HDL); bit error rate (BER); signal to noise ratio (SNR); Frequency Division Multiple Access (FDMA)

1. INTRODUCTION

This The first OFDM scheme dates back to 1966 when Robert W. Chang published his pioneering work on the synthesis of band-limited orthogonal signals for multi-channel data transmission. Orthogonal Frequency Division Multiplexing (OFDM) has been gaining year after year a well-deserved reputation, demonstrating its high data rate and robustness to wireless environments capabilities. In the multipath environment, broadband communications will suffer from frequency selective fading. OFDM is an attractive modulation scheme used in broadband wireless systems that encounter large delay spreads. OFDM avoids temporal equalization altogether, using a cyclic prefix technique with a small penalty in channel capacity. A VHSIC hardware description language (VHDL) is a very power tool used to describe behaviour of integrated circuits. We can simulate the transmitter & the receiver in the Communication system with help above mentioned tools.

2. ELEMENTS IN OFDM COMMUNICATION SYSTEM

2.1 OFDM

In OFDM communication system [1], serial binary input is applied to the scrambler & then channel coding is applied to improve the bit error rate. Depending on the application, the corresponding modulation scheme is applied (BPSK or QPSK).Now this modulated data is converted into size M parallel stream. Now using inverse FFT of size N, these M streams are modulated with different sub-carriers.

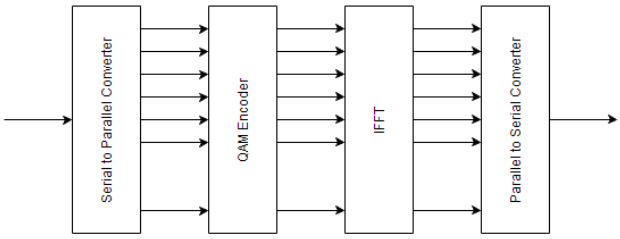

Fig.2.1 OFDM transmitter

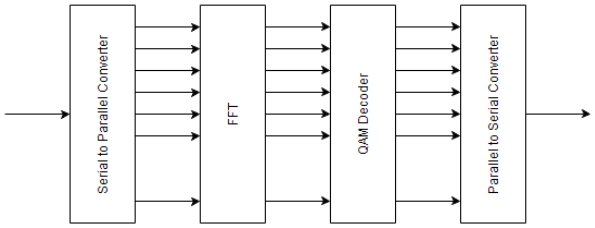

Fig.2.2 OFDM receiver

2.2 FPGA

In order to implement large circuits, it is convenient to use a type of chip that has a large logic capacity. A field-programmable gate arrays (FPGA) is a programmable logic device that supports implementations of relatively large logic circuits. FPGA is different from other logic technologies like CPLD and SPLD because FPGA do not contain AND or OR planes. Instead, FPGA consists of logic blocks for implementing the required functions. A FPGA contain three main types of resources: logic blocks, I/O blocks for connecting to the pins of the package, and interconnection wires and switches.

2.3 VHDL

VHDL is an acronym for VHSIC (Very High Speed Integrated Circuit) Hardware Description Language. It is intended for documenting and modeling digital systems ranging from a small chip to a large system. It can be used to model a digital system at any level of abstraction ranging from the architectural level down to the gate level. It allows the user to model the system as an interconnection of components. Test waveforms can be generated using the same constructs. All the above constructs may be combined to provide a comprehensive description of the system in a single model. The models written in VHDL can be verified using a VHDL simulator. It inherits extensive range of modeling capabilities that are difficult to understand. Fortunately, it is possible to quickly assimilate a core subset of the language that is easy and simple to understand without learning the complex features.

2.4 Advantages of OFDM

In general, OFDM systems have the following advantages:
(i) makes efficient use of the spectrum by allowing overlap; (ii) By dividing the channel into narrowband flat fading sub-channels, OFDM is more resistant to frequency selective fading than single carrier systems are; (iii) Eliminates ISI and IFI through use of a cyclic prefix; (iv) using adequate channel coding and interleaving one can recover symbols lost due to the frequency selectivity of the channel; (v) channel equalization becomes simpler than by using adaptive equalization techniques with single carrier systems; (vi) It is possible to use maximum likelihood decoding with reasonable complexity; (vii) OFDM is computationally efficient by using FFT techniques to implement the modulation and demodulation functions; (viii) Is less sensitive to sample timing offsets than single carrier systems are, and (ix) provides good protection against co-channel interference and impulsive parasitic noise [2].

3. VHDL EMULATION

3.1 Introduction

During this chapter the results obtained by testing the complete implemented OFDM system will be shown. The testing can be divided into two parts, a simulation part where all testing is done on the PC and a hardware part where testing is done in the hardware. First we will show the results obtained from the simulation part. All these simulations, as we said in the previous chapter, have been implemented using ModelSim 6.3f. Then, in the hardware part, the different equipment used for the testing of the OFDM system will be briefly introduced, and in addition, we will show the data obtained when using the FPGA device.

3.2 Simulation phase

For the simulation phase the testing is done on the PC using the ModelSim 6.3f. The implementation schemes used for the testing have already been introduced in the previous chapter so this section will be focused in the obtained results.

3.3 VHDL Emulation Results

Firstly the serial to parallel converter is used to convert the data from the serial form to the parallel form to introduce it to IFFT and it can be programmed using VHDL language.

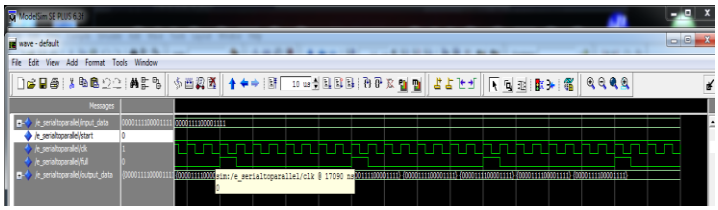

Fig 3.3.1 Serial to Parallel Converter

The next block is the Quadrature Amplitude Modulation (QAM) that is used as a simple type of complex digital modulation and as illustrated in fig.4.2

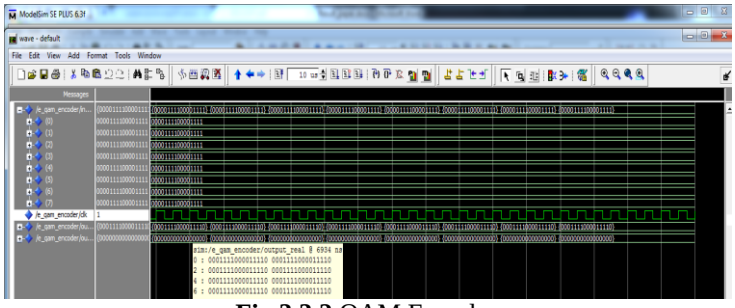

Fig 3.3.2 QAM Encoder

The Inverse Fast Fourier Transform (IFFT) transforms the signals from the frequency domain to the time domain; an IFFT converts a number of complex data points as illustrated in fig.4.3

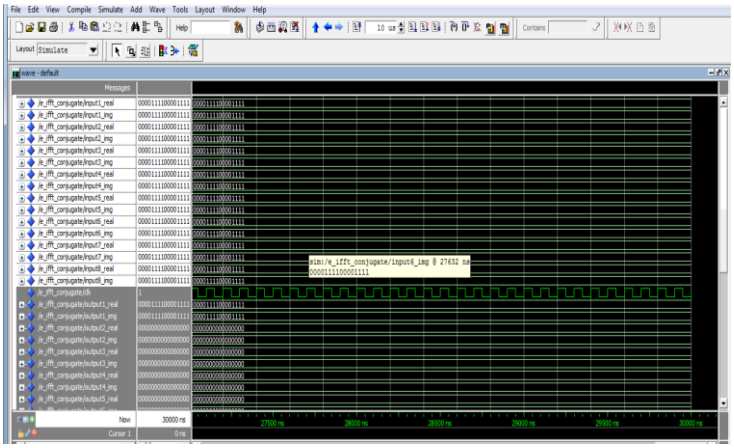

Fig 3.3.3 IFFT Block

Then data is again converted from parallel to serial and sent to receiver through communication channel. At receiver the data is again converted back from parallel to serial & given to the FFT block.

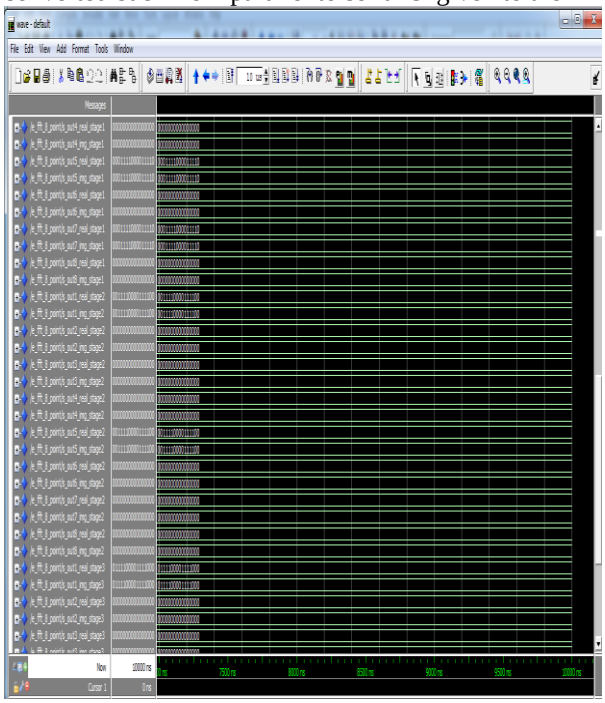

Fig 3.3.4 FFT Block

The ouput FFT block is given to the QAM decoder to decode the signal. The output of QAM decoder is as shown below.

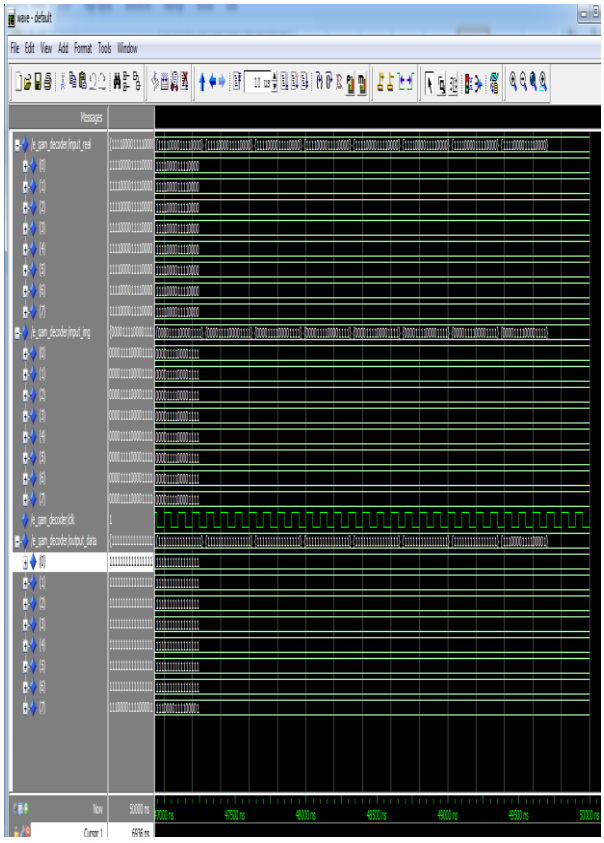

Fig 3.3.5 QAM decoder

4. Synthesis using altera quartus-ii

For synthesis of system Altera Quartus –II is used. The details of synthesis report is mentioned below.

Analysis & Synthesis Resource Usage Summary

	Resource	Usage
1	Total logic elements	100
2	-- Combinational with no register	48
3	-- Register only	4
4	-- Combinational with a register	48
5		
6	Logic element usage by number of LUT inputs	
7	-- 4 input functions	14
8	-- 3 input functions	31
9	-- 2 input functions	47
10	-- 1 input functions	4
11	-- 0 input functions	0
12		
13	Logic elements by mode	
14	-- normal mode	69
15	-- arithmetic mode	31
16	-- qfbk mode	0
17	-- register cascade mode	0
18	-- synchronous clear/load mode	4
19	-- asynchronous clear/load mode	0
20		
21	Total registers	52
22	Total logic cells in carry chains	32
23	I/O pins	18
24	Maximum fan-out node	testfsm1:U2|clk
25	Maximum fan-out	36
26	Total fan-out	345
27	Average fan-out	2.92

The details of logic elements used in the project is given in the above table.

5. Conclusion

So as mentioned above, we can conclude that the OFDM based FPGA systems are efficient. Also the high speed OFDM implementation is used for synthesis of this project. The output for each block is simulated & desired results are obtained. Also the simulated results on Model Sim 6.3f exactly matches with Altera Quartus-II on which code was synthesized.

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